REMARKS:

Claims 1, 3, and 5-25 are in the case and presented for consideration.

The Office has objected to the drawings because the elements in Fig. 1 have no labels. The Office has not cited any specific provision or rule that requires elements to include labels. Every element is provided with reference characters in accordance with 37 C.F.R. §1.84. However, in order to advance prosecution, elements 1-9 have been labeled in Fig. 1.

The Office has objected to the specification because section headings are missing. Applicants respectfully decline to add the headings as they are not required in accordance with MPEP §608.01(a).

Claim 1 was rejected under 35 U.S.C. 112, first paragraph. Claim 1 has been drafted to avoid the Office's §112 rejection and is believed to be in proper form.

Claims 1-23 were rejected under 35 U.S.C. 112, second paragraph. Claims 1-23 have been drafted to avoid the Office's §112 rejection and are believed to be in proper form.

Claims 1-3 were rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 3,373,404 to Webb.

Claim 1 was rewritten and now recites "summing the number of data bits written in the buffer memory" which is not taught or suggested by the cited prior art. Accordingly, claim 1 is believed to be patentable. Claims 2-23 depend from claim 1 and are also believed to be patentable for at least the same reasons.

New claim 24 recites "preparing said selected data bits so as to form an output data word, while utilizing a working bit register which contains m working bits and defines the output format, for output to a memory" which is not taught or suggested by

the prior art. Therefore, claim 24 is believed to be patentable.

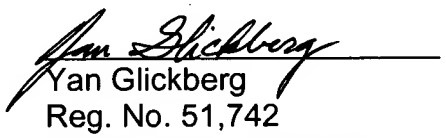
New claim 25 recites "writing said selected data bits into a buffer memory constructed as a shift register so that prior to the writing of a number of new data bits, the data bits that are already present are shifted over the number of new data bits", which is not taught or suggested by the prior art. Accordingly, new claim 25 is believed to be patentable.

Accordingly, the application and claims are believed to be in condition for allowance, and favorable action is respectfully requested. No new matter has been added.

If any issues remain which may be resolved by telephonic communication, the Examiner is respectfully invited to contact the undersigned at the number below, if such will advance the application to allowance.

Favorable action is respectfully requested.

Respectfully submitted,



Yan Glickberg
Reg. No. 51,742
Attorney for Applicants
(845) 359-7700

Dated: January 4, 2006

NOTARO & MICHALOS P.C.
100 Dutch Hill Road, Suite 110
Orangeburg, New York 10962-2100

Customer No. 21706

IN THE DRAWINGS:

Please amend the drawing of Fig. 1 by adding the label "data bit selection unit" for the box with reference number 1, the label "processor" for the box with reference number 2, the label "data word memory" for the box with reference number 3, the label "data word" for reference number 4, the label "selection bit register memory" for the box with reference number 5, the label "selection bit registers" for reference number 6, the label "buffer memory" for the box with reference number 7, the label "working bit register" for the box with reference number 8, and label "output data word" for the box with the reference number 9.